ONE TIME EXIT SCHEME

USN | | | | | | | | | | |

10EE764

Seventh Semester B.E. Degree Examination, April 2018
VLSI Circuits and Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain P – Well CMOS fabrication process with the help of necessary structures. **(08 Marks)**

b. Explain the action of enhancement mode transistor for different values of V_{gs} and V_{ds}. **(08 Marks)**

c. Compare CMOS and Bipolar technologies. **(04 Marks)**

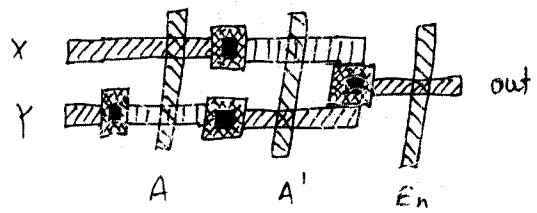
2 a. Explain the transfer plot of CMOS inverter with necessary expressions for V_{out} in each region. **(10 Marks)**

b. Explain various forms of Pull – up transistor as loads for inverter circuits. **(10 Marks)**

3 a. Draw the circuit diagram and stick diagram of two input NOR gate using CMOS logic. Use standard colour code / monochrome code. **(08 Marks)**

b. Draw the circuit diagram for the layout diagram shown in fig. Q3(b). **(08 Marks)**

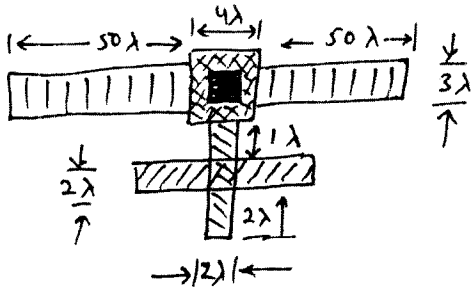
Fig.Q3(b)



c. List the λ – based design rules for contact cut. **(04 Marks)**

4 a. For the given multilayer MOS structure shown in fig.Q4(a), calculate the total capacitance in terms of C_g (5μm Technology). **(08 Marks)**

Fig.Q4(a)



Given : Metal 1 to substrate capacitance = 0.075 (Relative capacitance)
Polysilicon to substrate = 0.1.

b. Calculate ON resistance for nmos inverter with R_{Sn} = 10 kΩ, Z_{pu} = 4 and Z_{pd} = 1. **(06 Marks)**

c. Define Sheet resistance, Standard unit of capacitance and delay unit of time. **(06 Marks)**

PART – B

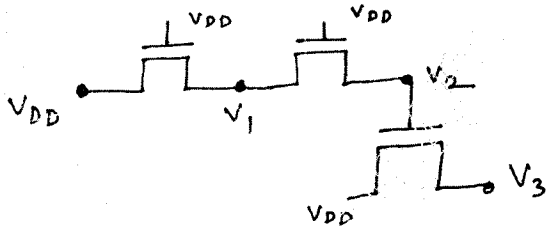
5 a. Find the scaling factors for the following parameters of MOS circuits :
i) Gate capacitance ii) Channel resistance iii) Saturation current
iv) Maximum operating frequency f_o v) Current density. **(10 Marks)**

b. What are the limitations of scaling current density and sub threshold current in MOS transistor? **(06 Marks)**

c. Explain Scaled nmos transistor, with neat sketch. **(04 Marks)**

6 a. Find V_1, V_2 and V_3 and justify your answer for the fig. Q6(a). **(06 Marks)**

Fig.Q6(a)



b. Explain 4 way multiplexer using nmos switch logic. **(06 Marks)**

c. Explain Four – bit dynamic shift register using nmos logic. **(08 Marks)**

7 a. List and explain some general considerations in design of digital systems. **(04 Marks)**

b. Explain 4 × 4 cross bar switch to implement barrel shifter, with neat sketch. **(06 Marks)**

c. Explain with neat sketch, design of various bus architecture linking sub – units. **(10 Marks)**

8 a. Explain the design steps for 4 – bit Adder. **(08 Marks)**

b. Explain the implementation of 4 – bit ALU functions using standard Adder's. **(08 Marks)**

c. Define Regularity in process design illustration. **(04 Marks)**

*****